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Single vacancy-oxygen complex defect and variable retention time phenomenon in silicon LSI memories

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Abstract: A two-level telegraph phenomenon, so-called "variable retention time (VRT)", is sometimes observed in silicon dynamic random access memories (DRAMs). It is believed to be related to a bistability of a single defect in silicon MOSFET and is recently highlighted as a fundamental issue in silicon LSI memories. We suggest that this telegraph phenomenon is caused by a single bistable vacancy-oxygen (*V*O) complex embedded in a silicon MOSFET of a DRAM VRT bit. We detected the *V*O complexes in DRAM cells by electrically detected magnetic resonance (EDMR). The location, electronic levels, and bistable nature of the *V*O complex are discussed in conjunction with the basic features of the VRT.

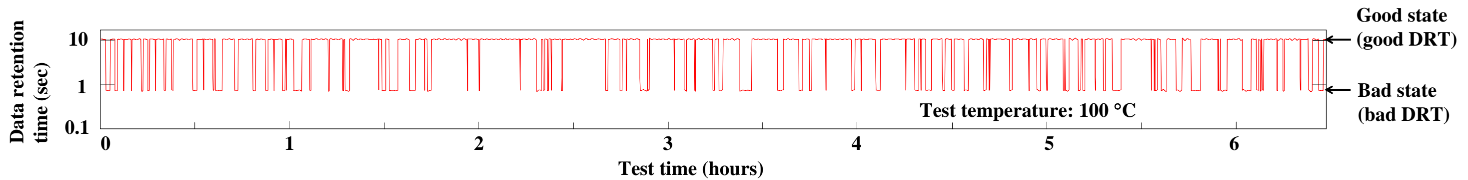

Fig. 1 Two-state variable retention time (VRT) in a DRAM bit.

What is the VRT? (Fig. 1): Two-state VRT is sometimes observed in DRAM bits. It exhibits a bistablity of the data retention time (DRT) [1]. The phenomenological origin of the VRT is a reversible change in junction leakage current of a silicon MOSFET [2]. The yield of the VRT is usually very low, but its impact is very big (the leakage current sometimes changes by a factor of 10 or larger). Because of its strict "telegraph" behavior, the VRT is believed to originate from ***a single bistable defect (the VRT defect)*** in a silicon MOSFET.

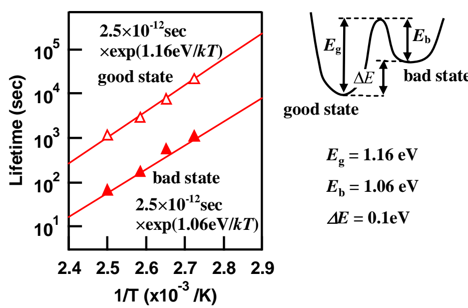

Fig. 2 Thermal activation of the VRT.

Bistability of the VRT defect (Fig. 2): The VRT is a thermally activated phenomenon. Restle *et al.* (IBM) [3] revealed that the VRT obeys a simple bistable energy diagram with "good state" and "bad state". Generally, good state = most stable, and bad state = metastable (i.e., $E_g > E_b$). The typical activation barrier is approximately 1 eV.

What types of defects are in silicon MOSFET? - EDMR study (Fig. 3): To directly observe defects related to the VRT, we carried out electrically detected magnetic resonance (EDMR) measurements on silicon MOSFETs in DRAMs (*n*-channel, gate length = 0.25-0.1 µm, a set of 10,000 MOSFETs). Every DRAM showed the same *silicon vacancy-oxygen (VO) complex* defects in EDMR spectra. These were already assigned to either large *V*O complex or V_2O_x complex [4]. Both defect signals were very sensitive to the gate voltage, indicating that these defects are located in the near surface region close to the gate electrode. We propose that the minor type, V_2O_x complex, is the VRT defect.

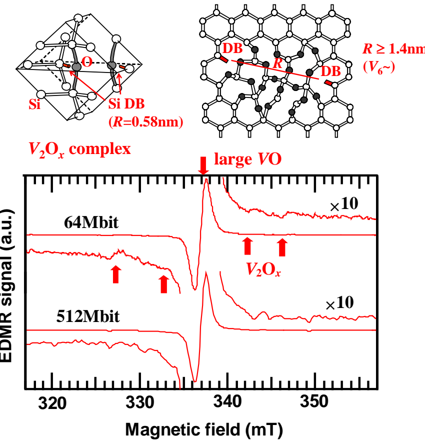

Fig. 3 EDMR spectra of 10,000 DRAM cells.

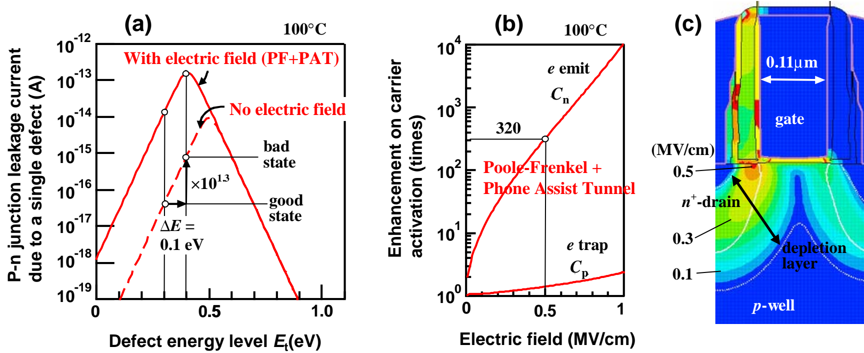

Fig. 4 Defect vs. junction leakage current under a strong electric field.

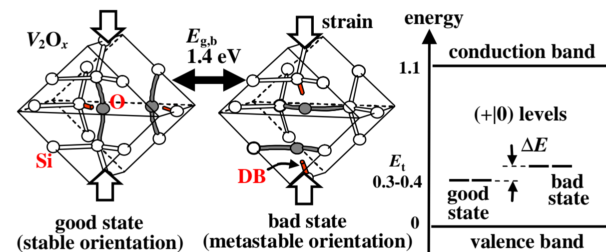

Fig. 5 V_2O_x defect model

Can really a single defect generate a big leakage? – Yes, it is possible (Fig. 4): Usually leakage current from a single defect is very small (< 10 fA) [***dashed line in (a)***, calculated by the SRH formula with C_n=1×10^{-14}cm^2 , C_p=1×10^{-15}cm^2]. But, a strong electric field can drastically enhance the leakage by a factor of 320 at 0.5 MV/cm [***C_n in (b)***]. Such electric field can be applied to a V_2O_x complex located at the near surface gate-drain boundary [see ***(c)***]. Finally, such a special V_2O_x can generate a very high leakage current over 100 fA [***solid line in (a)***, calculated using C_n=300×10^{-14}cm^2 , C_p=1×10^{-15}cm^2]. The two bistable states of the VRT can be reproduced by $E_t = E_V$ +0.3-0.4eV, ΔE= 0.1eV.

Energy level and bistability of V_2O_x (Fig. 5): The V_2O_x defect has two silicon dangling bonds (S=1) which generate two (+|0) levels close to the energy levels of the VRT defect: $E_t = E_V$ +0.3-0.4 eV [1]. We ascribe the origin of the bistability as a strong lattice strain in Si LSI devices. Under a strong strain, one orientation should be most stable while the other orientation should be metastable. The activation barrier for the reorientation was approximately 1.4 eV [5], which is consistent with that of the VRT.

References:

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